IN THE DRAWINGS

Figure 1 is being amended to include the designation of Prior Art. A replacement sheet is enclosed for entry in the file.

REMARKS

Claims 1-31 are pending. Independent claims 1, 19, and 27 were rejected under 35 U.S.C. 102(b) as being anticipated by Owen (USPN 4,876,660). Claims 5, 11, and 14 have been amended to address informalities.

Owen describes a multiplier accumulator architecture. "When two 16-bit operands are multiplied, the product output from multiplier 30 and input to adder port 36 is 32 bits wide. Summation of this number with another number of a comparable number of bits commonly produces overflow bits. Most conventional 16.times.16 bit multiplier-accumulators provide an extended 3-bit register above the most significant 16-bit (MSW) register to handle these added bits. The preferred embodiment adds eight more significant or carry bits. This will accommodate a minimum of 256 summations and up to 1024 summations with normally distributed data. One additional bit is added as a most-significant or overflow bit." (Column 9, Lines 25-37)

"The adder output is accordingly structured to output a total of 41 bits. This includes 32 bits for the sum of the number of the bits in each of the operands, 8 carry bits and one additional bit, for a total of 41 bits. The accumulators are likewise structured to input and output a 41-bit result. The accumulators are structured in the form of an extended 8-bit register for receiving the eight least significant bits (bits 0-7); a 16-bit register for receiving bits 8-23 and a 17-bit register for receiving the most significant bits 24-39 and overflow or carry bit 40. The data input at the adder ports is always aligned, upon input, with its least significant bit in the least significant bit position of the adder array. The Z result output from the adder is similarly aligned so that its least significant bit is positioned in the least significant bit position of the selected accumulator." (Column 9, Lines 38-47)

The Examiner argues that that the adder 34 in Owen is an arithmetic logic unit and the accumulators 40 and 42 in Owen are a plurality of registers. The Applicants respectfully disagree. An adder is not an arithmetic logic unit. Although it is acknowledged that one of the functions an arithmetic logic unit can perform is addition, an arithmetic logic unit is not merely an adder. An arithmetic logic unit is a significant component of a processor and is operable to perform addition, subtraction, bit shifting operations, and logic operations, not merely addition. The Examiner may attempt to argue that the logic described in Owen also includes a multiplier.

However, the multiplier does not write data and carry flag information to one of the plurality of registers.

Furthermore, the independent claims have been amended to recite a "processor register" and an arithmetic logic unit "operable to read and write carry flag information data and information." Although it is acknowledge that Owens describes an adder that provides output values to accumulators, the Owen accumulator is not a processor register and the accumulator can not be read and written by the arithmetic logic unit. Although the accumulator is implemented using registers, the accumulator is not a processor register that allows reading and writing of carry flag information and data information by an arithmetic logic unit. At most, the accumulator allows writes by an adder.

In light of the above remarks, the rejections to the independent claims are believed overcome for at least the reasons noted above. Applicants believe that all pending claims are allowable in their present form. Please feel free to contact the undersigned at the number provided below if there are any questions, concerns, or remaining issues.

Respectfully submitted,
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